DATA SHEET

I²C BUS

SAB9082
NTSC Picture-In-Picture (PIP) controller

Preliminary specification
Supersedes data of 1999 Feb 18
File under Integrated Circuits, IC02

1999 Nov 12

Philips
Semiconductors

PHILIPS

NTSC Picture-In-Picture (PIP) controller   SAB9082

FEATURES

- Double window Picture-in-Picture (PIP) in interlaced or non-interlaced mode at 8-bit resolution
- Internal 1-Mbit DRAM
- Three 8-bit Analog-to-Digital Converters (ADCs) (7-bit performance) with clamp circuit for each acquisition channel
- One PLL which generates the line-locked clocks for the subchannel
- One PLL which generates the line-locked clocks for the main and display channels
- Three 8-bit Digital-to-Analog Converters (DACs)
- Linear zoom in both horizontal and vertical directions for the subchannel
- Linear zoom in horizontal direction for the main channel
- Three multistandard PIP modes are available.

GENERAL DESCRIPTION

The SAB9082 is an NTSC PIP controller which can be used in double window applications. The SAB9082 inserts one or two live video signals with reduced size into another live video signal. The incoming video signals are expected to be analog baseband signals.

The conversion to the digital environment is done on chip with ADCs. Processing and storage of the video data is done entirely in the digital domain. The conversion back to the analog domain is done by means of DACs.

Internal clocks are generated by PLLs which lock on to the applied horizontal and vertical syncs.

The main input channel is compressed horizontally by a factor of two and directly fed to the output. After compression, a horizontal expansion of two is possible for the main channel.

The subchannel is also compressed horizontally by a factor of two but stored in memory before it is fed to the outputs.

The SAB9082 can also create three multistandard PIP modes, one with three PIPs placed in a column (MP3) and two with two columns of three PIPs (MP6, MP6S). The reduction factors of these PIPs are horizontal $\frac{1}{4}$ and vertical $\frac{1}{3}$. In the first two modes, the column(s) can be placed on the left or right side of the screen.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		–	50	–	mA
I_{DDA}	analog supply current		140	165	210	mA
PLL						
$f_{clk(sys)}$	system clock frequency	$1792 \times f_{HSYNC}$	–	28	–	MHz
B_{loop}	loop bandwidth		–	4	–	kHz
t_{jitter}	short-term stability	peak-to-peak jitter for 64 µs	–	–	4	ns
ζ	damping factor		–	0.7	–	

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9082H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 $\times$ 20 $\times$ 2.8 mm	SOT317-2
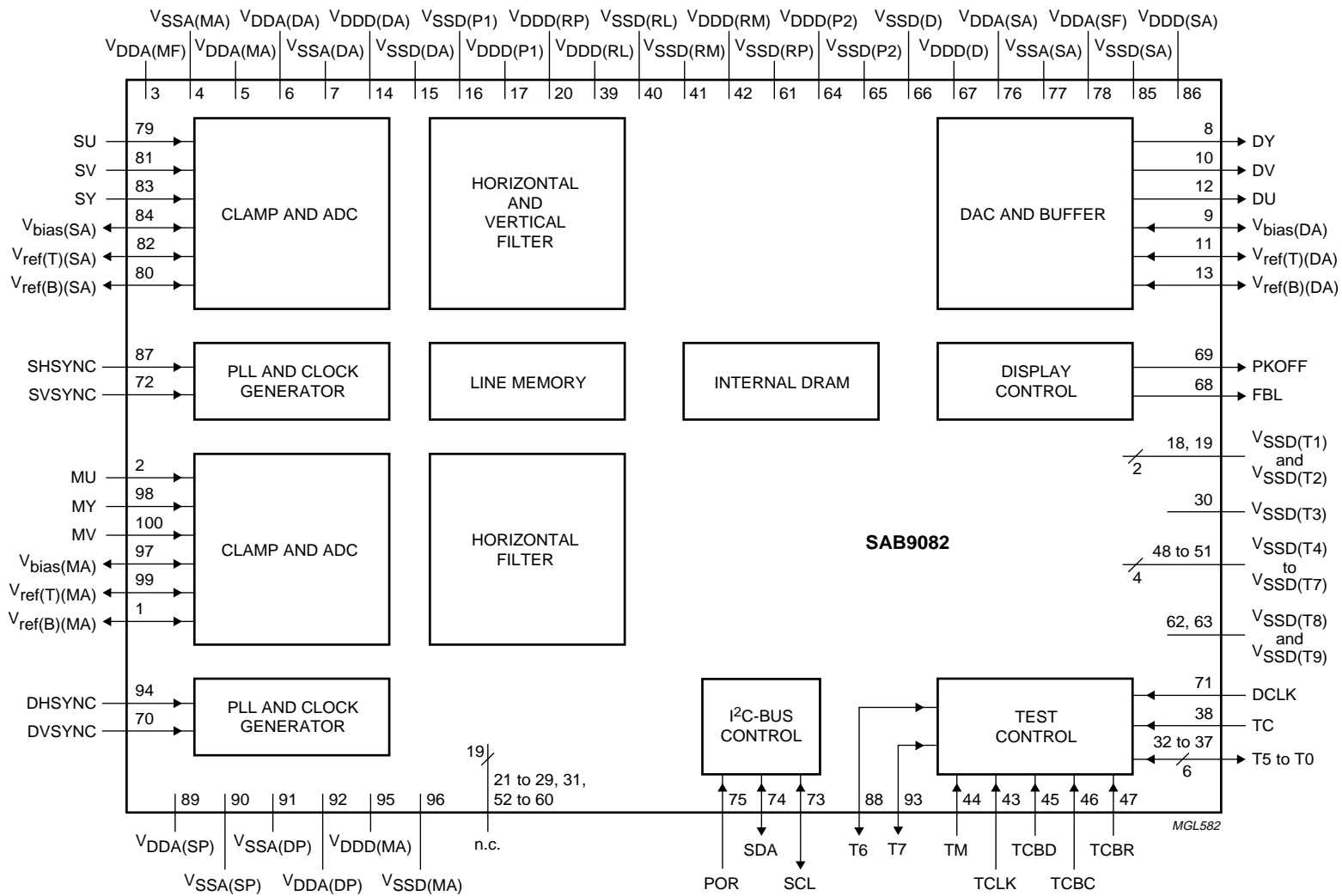
BLOCK DIAGRAM

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$V_{ref(B)(MA)}$	1	I/O	analog bottom reference voltage for main channel ADCs
MU	2	I	analog U input for main channel
$V_{DDA(MF)}$	3	S	analog supply voltage for main channel front-end buffers
$V_{SSA(MA)}$	4	S	analog ground for main channel ADCs
$V_{DDA(MA)}$	5	S	analog supply voltage for main channel ADCs
$V_{DDA(DA)}$	6	S	analog supply voltage for DACs
$V_{SSA(DA)}$	7	S	analog ground for DACs
DY	8	O	analog Y output of DAC
$V_{bias(DA)}$	9	I/O	input/output analog bias reference voltage for DACs
DV	10	O	analog V output of DAC
$V_{ref(T)(DA)}$	11	I/O	input/output analog top reference voltage for DACs
DU	12	O	analog U output of DAC
$V_{ref(B)(DA)}$	13	I/O	analog bottom reference voltage for DACs
$V_{DDD(DA)}$	14	S	digital supply voltage for DACs
$V_{SSD(DA)}$	15	S	digital ground for DACs
$V_{SSD(P1)}$	16	S	digital ground for periphery
$V_{DDD(P1)}$	17	S	digital supply voltage for periphery
$V_{SSD(T1)}$	18	S	digital ground for test
$V_{SSD(T2)}$	19	S	digital ground for test
$V_{DDD(RP)}$	20	S	digital supply voltage for memory periphery
n.c.	21 to 29	–	not connected
$V_{SSD(T3)}$	30	S	digital ground for test
n.c.	31	–	not connected
T5	32	I/O	test data input/output bit 5 (CMOS levels)
T4	33	I/O	test data input/output bit 4 (CMOS levels)
T3	34	I/O	test data input/output bit 3 (CMOS levels)
T2	35	I/O	test data input/output bit 2 (CMOS levels)
T1	36	I/O	test data input/output bit 1 (CMOS levels)
T0	37	I/O	test data input/output bit 0 (CMOS levels)
TC	38	I	test control input (CMOS levels)
$V_{DDD(RL)}$	39	S	digital supply voltage for memory logic
$V_{SSD(RL)}$	40	S	digital ground for memory logic
$V_{SSD(RM)}$	41	S	digital ground for memory core
$V_{DDD(RM)}$	42	S	digital supply voltage for memory core
TCLK	43	I	test clock input (CMOS levels)
TM	44	I	test mode input (CMOS levels)
TCBD	45	I	test control block data input (CMOS levels)
TCBC	46	I	test control block clock input (CMOS levels)
TCBR	47	I	test control block reset input (CMOS levels)
$V_{SSD(T4)}$ to $V_{SSD(T7)}$	48 to 51	S	digital ground for test

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SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	52 to 60	–	not connected
$V_{SSD(RP)}$	61	S	digital ground for memory periphery
$V_{SSD(T8)}$ and $V_{SSD(T9)}$	62 and 63	S	digital ground for test
$V_{DDD(P2)}$	64	S	digital supply voltage for periphery
$V_{SSD(P2)}$	65	S	digital ground for periphery
$V_{SSD(D)}$	66	S	digital ground for digital core
$V_{DDD(D)}$	67	S	digital supply voltage for digital core
FBL	68	O	fast blanking control signal output (CMOS levels; +5 V tolerant)
PKOFF	69	O	peak off control signal output (CMOS levels; +5 V tolerant)
DVSYNC	70	I	vertical sync display channel input (CMOS levels; +5 V tolerant)
DCLK	71	I	test clock input (28 MHz; CMOS levels)
SVSYNC	72	I	vertical sync for subchannel input (CMOS levels; +5 V tolerant)
SCL	73	I/O	input/output serial clock (I^2C-bus; CMOS levels; +5 V tolerant)
SDA	74	I/O	input/output serial data/acknowledge output (I^2C-bus; +5 V tolerant)
POR	75	I	power-on reset input (CMOS levels; pull-up resistor connected to V_{DD})
$V_{DDA(SA)}$	76	S	analog supply voltage for subchannel ADCs
$V_{SSA(SA)}$	77	S	analog ground for subchannel ADCs
$V_{DDA(SF)}$	78	S	analog supply voltage for subchannel front-end buffers and clamps
SU	79	I	analog U input for subchannel
$V_{ref(B)(SA)}$	80	I/O	input/output analog bottom reference voltage for subchannel ADCs
SV	81	I	analog V input for subchannel
$V_{ref(T)(SA)}$	82	I/O	input/output analog top reference voltage for subchannel ADCs
SY	83	I	analog Y input for subchannel
$V_{bias(SA)}$	84	I/O	analog bias reference voltage for subchannel ADCs
$V_{SSD(SA)}$	85	S	digital ground for subchannel ADCs
$V_{DDD(SA)}$	86	S	digital supply voltage for subchannel ADCs
SHSYNC	87	I	horizontal sync input for subchannel ($V_i < V_{SHSYNC}$)
T6	88	I/O	test data input/output bit 7 (CMOS levels)
$V_{DDA(SP)}$	89	S	analog supply voltage for subchannel PLL
$V_{SSA(SP)}$	90	S	analog ground for subchannel PLL
$V_{SSA(DP)}$	91	S	analog ground for display channel PLL
$V_{DDA(DP)}$	92	S	analog supply voltage for display channel PLL
T7	93	I/O	test data input/output bit 6 (CMOS levels)
DHSYNC	94	I	horizontal sync input for display channel ($V_i < V_{DHSYNC}$)
$V_{DDD(MA)}$	95	S	digital supply voltage for main channel ADCs
$V_{SSD(MA)}$	96	S	digital ground for main channel ADCs
$V_{bias(MA)}$	97	I/O	analog bias reference voltage for main channel ADCs
MY	98	I	analog Y input for main channel
$V_{ref(T)(MA)}$	99	I/O	analog top reference voltage for main channel ADCs
MV	100	I	analog V input for main channel

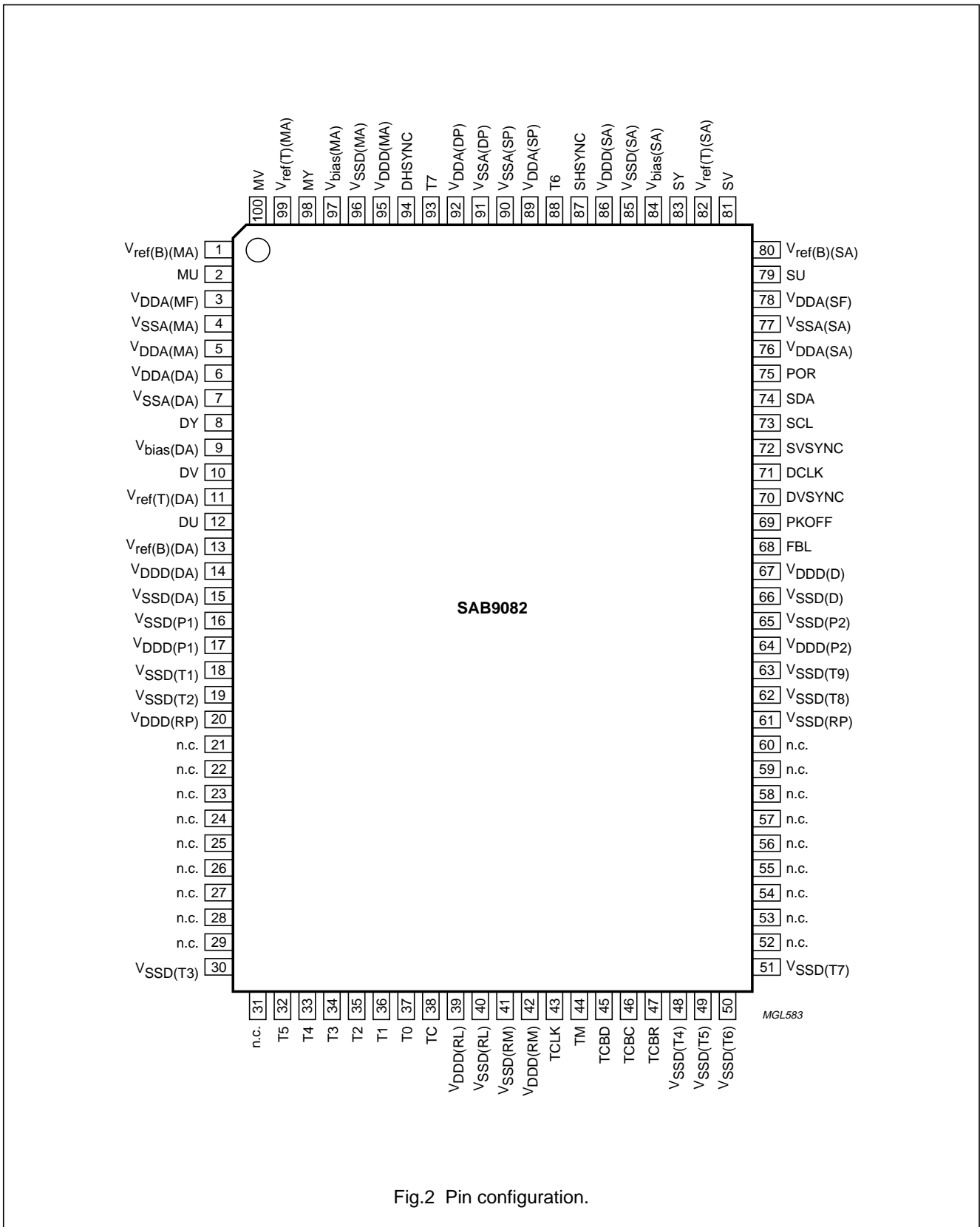NTSC Picture-In-Picture (PIP) controller

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Top pins (100–81):
100 MV
99 $V_{ref(T)(MA)}$
98 MY
97 $V_{bias(MA)}$
96 $V_{SSD(MA)}$
95 $V_{DDD(MA)}$
94 DHSYNC
93 T7
92 $V_{DDA(DP)}$
91 $V_{SSA(DP)}$
90 $V_{SSA(SP)}$
89 $V_{DDA(SP)}$
88 T6
87 SHSYNC
86 $V_{DDD(SA)}$
85 $V_{SSD(SA)}$
84 $V_{bias(SA)}$
83 SY
82 $V_{ref(T)(SA)}$
81 SV

Left pins (1–30):
1 $V_{ref(B)(MA)}$
2 MU
3 $V_{DDA(MF)}$
4 $V_{SSA(MA)}$
5 $V_{DDA(MA)}$
6 $V_{DDA(DA)}$
7 $V_{SSA(DA)}$
8 DY
9 $V_{bias(DA)}$
10 DV
11 $V_{ref(T)(DA)}$
12 DU
13 $V_{ref(B)(DA)}$
14 $V_{DDD(DA)}$
15 $V_{SSD(DA)}$
16 $V_{SSD(P1)}$
17 $V_{DDD(P1)}$
18 $V_{SSD(T1)}$
19 $V_{SSD(T2)}$
20 $V_{DDD(RP)}$
21 n.c.
22 n.c.
23 n.c.
24 n.c.
25 n.c.
26 n.c.
27 n.c.
28 n.c.
29 n.c.
30 $V_{SSD(T3)}$

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Right pins (80–51):
80 $V_{ref(B)(SA)}$
79 SU
78 $V_{DDA(SF)}$
77 $V_{SSA(SA)}$
76 $V_{DDA(SA)}$
75 POR
74 SDA
73 SCL
72 SVSYNC
71 DCLK
70 DVSYNC
69 PKOFF
68 FBL
67 $V_{DDD(D)}$
66 $V_{SSD(D)}$
65 $V_{SSD(P2)}$
64 $V_{DDD(P2)}$
63 $V_{SSD(T9)}$
62 $V_{SSD(T8)}$
61 $V_{SSD(RP)}$
60 n.c.
59 n.c.
58 n.c.
57 n.c.
56 n.c.
55 n.c.
54 n.c.
53 n.c.
52 n.c.
51 $V_{SSD(T7)}$

Bottom pins (31–50):
31 n.c.
32 T5
33 T4
34 T3
35 T2
36 T1
37 T0
38 TC
39 $V_{DDD(RL)}$
40 $V_{SSD(RL)}$
41 $V_{SSD(RM)}$
42 $V_{DDD(RM)}$
43 TCLK
44 TM
45 TCBD
46 TCBC
47 TCBR
48 $V_{SSD(T4)}$
49 $V_{SSD(T5)}$
50 $V_{SSD(T6)}$

MGL583

Fig.2 Pin configuration.

NTSC Picture-In-Picture (PIP) controller
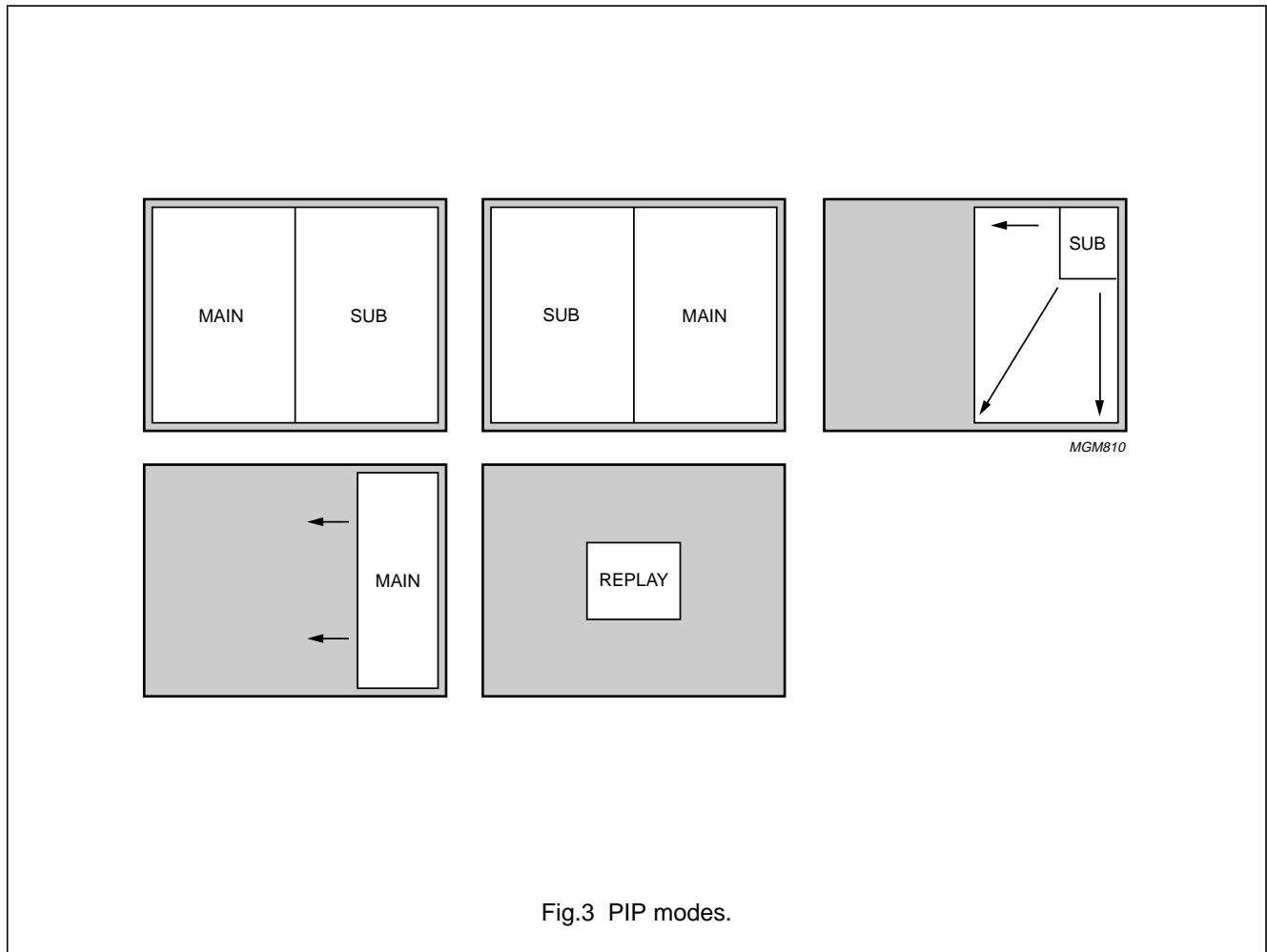
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FUNCTIONAL DESCRIPTION

Acquisition

The internal pixel rate is 28 MHz for the Y, U and V channels. It is expected that the bandwidth of the input signals will be limited to 4.5 MHz for the Y input and 1.125 MHz for the U and V inputs. Inset synchronization is achieved via the acquisition HSYNC and VSYNC pins of the main channel. The display is driven by the main channel clock.

The starting-point of the acquisition can be controlled with the acquisition fine positioning added to a system constant. With a nominal input f_{HSYNC} and standard NTSC signals, 1408 samples (active video) are acquired and processed by the SAB9082. Here, the nominal input f_{HSYNC} results in a nominal system clock frequency of $1792 \times f_{HSYNC}$ (approximately 28 MHz).

PIP modes

Fig.3 PIP modes.
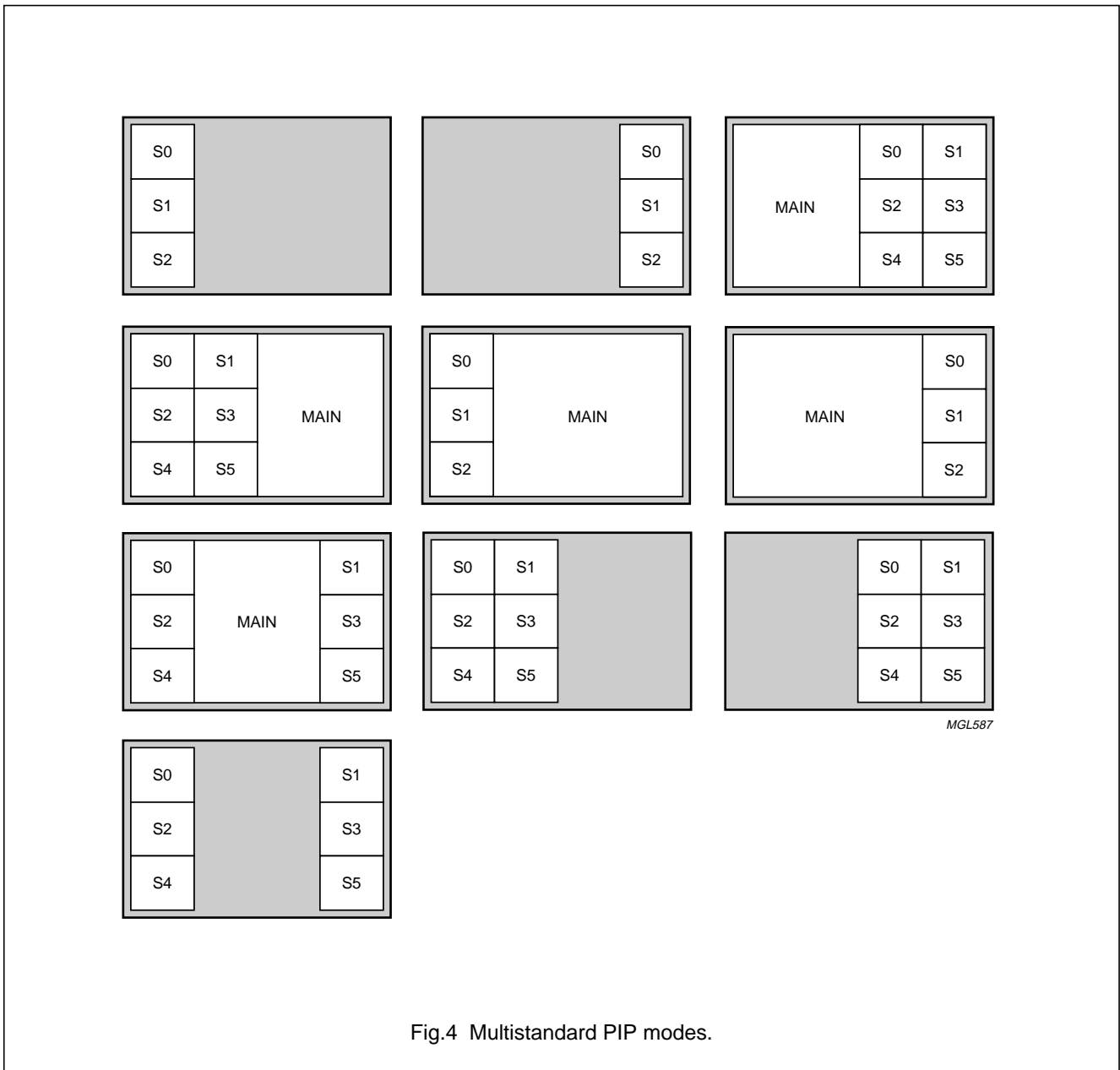
Fig.4 Multistandard PIP modes.

I²C-bus description

The I²C-bus provides bidirectional 2-line communication between different ICs. The SDA line is the serial data line and the SCL the serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device.

Data transfer may be initiated only when the bus is not busy. The SAB9082 has the I²C-bus address 2CH. Valid subaddresses are 00H to 18H, registers 15H to 18H are reserved for future extensions.

I²C-bus control is according to the I²C-bus protocol: first, a START sequence must be put on the I²C-bus. Then, the I²C-bus address of the circuit must be sent, followed by a subaddress. After this sequence, the data of the subaddresses must be sent. An auto-increment function gives the option of sending data of the incremented subaddresses until a STOP sequence is sent. Table gives an overview of the I²C-bus addresses. The data bits that are not used should be set to zero.

Table 1 Overview of I²C-bus addresses

For a description of the various data bits, see the following pages

SUB ADDRESS	DATA BYTES							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00H	MPIPON	SPIPON	S1FLD	SFreeze	DNonint	PipMode2	PipMode1	PipMode0
01H	SHBlow1	SHBlow0	SHRed5	SHRed4	SHRed3	SHRed2	SHRed1	SHRed0
02H	SVBlow	SVRed6	SVRed5	SVRed4	SVRed3	SVRed2	SVRed1	SVRed0
03H	BGVfp3	BGVfp2	BGVfp1	BGVfp0	BGHfp3	BGHfp2	BGHfp1	BGHfp0
04H	SDHfp7	SDHfp6	SDHfp5	SDHfp4	SDHfp3	SDHfp2	SDHfp1	SDHfp0
05H	SDVfp7	SDVfp6	SDVfp5	SDVfp4	SDVfp3	SDVfp2	SDVfp1	SDVfp0
06H	SHPic7	SHPic6	SHPic5	SHPic4	SHPic3	SHPic2	SHPic1	SHPic0
07H	SVPic7	SVPic6	SVPic5	SVPic4	SVPic3	SVPic2	SVPic1	SVPic0
08H	MAHfp3	MAHfp2	MAHfp1	MAHfp0	SAHfp3	SAHfp2	SAHfp1	SAHfp0
09H	SAVfp7	SAVfp6	SAVfp5	SAVfp4	SAVfp3	SAVfp2	SAVfp1	SAVfp0
0AH	DUVPol	DVSPol	DFPol	DHsync	SUVPol	SVSPol	SFPol	SHsync
0BH	MainFidPos7	MainFidPos6	MainFidPos5	MainFidPos4	MainFidPos3	MainFidPos2	MainFidPos1	MainFidPos0
0CH	SubFidPos7	SubFidPos6	SubFidPos5	SubFidPos4	SubFidPos3	SubFidPos2	SubFidPos1	SubFidPos0
0DH	BGOn	BOn	MFidPOn	SFidPOn	Prio	AlgOff	SFBlkPkOff1	SFBlkPkOff0
0EH	BSel1	BSel0	SBBrt1	SBBrt0	–	SBCol2	SBCol1	SBCol0
0FH	–	–	SLSel5	SLSel4	SLSel3	SLSel2	SLSel1	SLSel0
10H	I2CHold	SV1	SDSel5	SDSel4	SDSel3	SDSel2	SDSel1	SDSel0
11H	MDHfp7	MDHfp6	MDHfp5	MDHfp4	MDHfp3	MDHfp2	MDHfp1	MDHfp0
12H	MDVfp7	MDVfp6	MDVfp5	MDVfp4	MDVfp3	MDVfp2	MDVfp1	MDVfp0
13H	MHBlow	SV2	MHRed5	MHRed4	MHRed3	MHRed2	MHRed1	MHRed0
14H	–	VBWidth2	VBWidth1	VBWidth0	–	HBWidth2	HBWidth1	HBWidth0
15H to 18H	all bits are reserved							

MPIPON (DOUBLE WINDOW)

Bit MPIPON is used to switch the main channel PIP on (logic 1) or off (logic 0).

SPIPON

Bit SPIPON is used to switch the subchannel PIPs on (logic 1) or off (logic 0).

PRIO

The priority bit decides whether the main channel PIP (Prio set to logic 0) or the subchannel PIP (Prio set to logic 1) will be on top when both PIPs overlap.

S1FLD

If S1FLD is set to logic 0, two fields are used for the live PIP. When a 50/60 Hz or a 60/50 Hz mode is detected, the SAB9082 automatically switches to the 1-Field mode (1-Field resolution vertically).

If S1FLD is set to logic 1, only one field is used. This causes joint line errors but saves memory. This bit should not be set in normal modes.

SFREEZE

With SFreeze set to logic 1, the current live subchannel PIP will be frozen. If set to logic 0, it is unfrozen.

ALGOFF

In double window mode, precautions are taken to prevent a joint line error. Under some conditions, this feature should be switched off. This can be realized by setting this bit to logic 1. Normally, bit AlgOff should be set to logic 0.

DNONINT

In normal mode (this bit is logic 0), the SAB9082 calculates whether a signal is non-interlaced and reacts accordingly. With bit DNonint set to logic 1, the display channel is forced into the non-interlaced mode. In the non-interlaced mode, only one field is used during the processing of the PIPs.

PIPMODE

Byte PipMode determines the PIP modes for the SAB9082 are shown in Table 2.

Table 2 PIP modes

PipMode<2:0>	MODE
000	double window mode
001	replay PIP
010	multistandard PIP 3
011	multistandard PIP 6
100	reserved
111	multistandard PIP 6 split

SHRED AND SVRED (DOUBLE WINDOW)

Bits SHRed<5:0> and SVRed<6:0> determine the reduction factors in the double window mode.

The horizontal reduction is equal to SHRed/96; the vertical reduction is equal to SVRed/96. SHRed should lie in the range from 0 to 48; if set to logic 0, the PIP is off. SVRed should lie in the range from 0 to 96; if set to logic 0, the PIP is off.

When the horizontal reduction factor is 48/96, 704 samples are processed. The horizontal reduction factor is linear; therefore, when it is 24/96, 352 samples are processed. The same holds for the vertical reduction factor but then with the number of lines. For NTSC, the number of processed lines can be calculated from SVRed/96 × 228 lines.

SHRED AND SVRED (REPLAY)

In the replay mode, the range of SHRed and SVRed is limited as follows: SHRed = 12; SVRed = 24, 16 or 12. This leads to a fixed horizontal reduction factor of $\frac{1}{8}$; and to a variable vertical reduction factor of $\frac{1}{4}$, $\frac{1}{6}$ or $\frac{1}{8}$. Note that the resulting replay PIP can be expanded by using SHBlow and/or SVBlow.

SHPIC AND SVPIC (MULTISTANDARD PIP MODES)

Bytes SHPic and SVPic control the picture size in the multistandard PIP modes. The horizontal range is 256 steps of four 28 MHz clock periods. The vertical range is 256 steps of one line/field.

In the double window and replay modes, the picture size is determined by the reduction factors (SHRed and SVRed) and bits HBlow and VBlow.

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BGHFP AND BGVFP

These bits control the horizontal and vertical positioning of the PIP configuration on the screen. The horizontal range is adjustable in 16 steps of four 28 MHz clock periods. The vertical range is 16 steps of 1 line/field.
The background colour can be adjusted with bits BSel, SBBrt and SBCol.

SDHFP AND SDVFP

These bytes control the horizontal and vertical positioning of the subchannel PIPs on the screen. The horizontal range is 256 steps of eight 28 MHz clock periods.
The vertical range is 256 steps of 1 line/field.

MAHFP, SAHFP AND SAVFP

Bits MAHfp<3:0>, bits SAHfp<3:0> and byte SAVfp control the horizontal and vertical inset starting-points of the acquired data. The horizontal range is 16 steps of eight 28 MHz clock periods when SV2 is set to logic 1. When SV2 is set to logic 0, the horizontal range is restricted to eight steps. The vertical range is 256 steps of 1 line/field.

DUVPOL, DVSPOL, DFPOL AND DHSYNC

These bits control the PLL/deflection settings. With DUVPol, the polarity of the border UV signals can be inverted when the deflection circuit after the SAB9082 expects inverted signals. With DVSPol set to logic 0, the SAB9082 triggers on positive edges of the DVSYNC. If DVSPol is set to logic 1, it triggers on negative edges. Bit DFPol can invert the field ID of the incoming fields. Bit DHsync determines the timing of the DHSYNC pulse. If it is set to logic 0, a burstkey is expected and if it is set to logic 1, a horizontal sync is expected at pin DHSYNC.

SUVPOL, SVSPOL, SFPOL AND SHSYNC

These bits control the PLL/decoder settings. With SUVPol, the polarity of the video UV signals can be inverted when the decoder circuit before the SAB9082 emits inverted signals. With SVSPol set to logic 0, the SAB9082 triggers on positive edges of the SVSYNC. If it is set to logic 1, it triggers on the negative edges. Bit SFPol can invert the field ID of the incoming fields. Bit SHsync determines the timing of the SHSYNC pulse. If it is set to logic 0, a burstkey is expected and if it is set to logic 1, a horizontal sync is expected at pin SHSYNC.

MFIDPON AND SFIDPON

Bits MFidPOn (main field identification position on) and SFidPOn (subfield identification position on) enable the field identification position fine tuning. The default value is off (logic 0), no fine positioning. When on (logic 1), the field identification position is determined by the value of MainFidPos and SubFidPos.

BGON

Bit BGOn determines whether the background is visible. The background has a size of 720 pixels and 240 lines for NTSC. The background colour can be adjusted with bits BSel, SBBrt and SBCol.

BON, SBBRT, SBCOL AND BSEL

Bit BOn can switch the sub-borders on (logic 1) or off (logic 0). Bits SBBrt<1:0> and SBCol<2:0> set the brightness and colour type of the selected border. The brightness is set in four levels of 30%, 50%, 70% and 100% IRE. The colour type is one of black (grey), blue, red, magenta, green, cyan, yellow or white (grey).For black and white, a finer scale is available Bits BSel<1:0> select which colour is set, background or border, see Table 3.

Table 3 BSel modes

BSel<1:0>	BORDER COLOUR SET
00	main
01	sub
10	background
11	sub-border select

MDHFP AND MDVFP

These bytes control the horizontal and vertical positioning of the main PIP on the screen. The horizontal range is 256 steps of eight 28 MHz clock periods. The vertical range is 256 steps of 1 line/field.

MHRED

Bits MHRed<5:0>, in a range from 0 to 48, determine the horizontal reduction factor MHRed/96. If they are set to logic 0, the PIP is off. If they are set to the maximum value of 48, the horizontal reduction factor is 0.5.

SHBLOW AND SVBLOW (REPLAY MODE)

Bits SHBlow<1:0> and bit SVBlow are used in the replay mode. These bits can expand a pixel on the display side by a factor two (01) or four (11) in the horizontal direction (SHBlow) and a factor of two (1) in the vertical direction (SVBlow). Zero values indicate no expansion.

MHBLOW

Bit MHBlow can expand the main picture by a factor of two in the horizontal direction.

SLSEL (REPLAY MODE)

In the replay PIP mode, bits SLSel<5:0> determine at which memory location the PIP data is written, the range depends on the memory usage for each PIP.
The maximum number of PIPs that can be stored in NTSC mode is 42.

SLSEL (MULTISTANDARD PIP MODES)

Bits SLSel<5:0> select which of the PIPs in a multistandard PIP mode is live. In MP3 modes, SLSel must be in the range from 0 to 2. In all MP6 modes, SLSel must be in the range from 0 to 5.

SDSEL (REPLAY MODE)

Bits SDSel<5:0> select which PIP is read from memory. Valid numbers are dependent on the maximum value of SLSel.

SFBLKPKOFF

Bits SFBlkPkOff<1:0> shift signals FBL and PKOFF with respect to the YUV output, by half pixels, see Table 4.

Table 4 Shifts of FBLK and PKOff

SFBlkPkOff<1:0>	SHIFT OF FBL AND PKOFF
00	no shift
01	+0.5 pixel
10	−0.5 pixel
11	−1 pixel

I2CHOLD

Bit I2CHold controls the updating of the I2C-bus controlled function towards the PIP. If set to logic 1, some updates are on hold until the bit is set to logic 0. At the next main Vsync, all settings are passed to the PIP functions.

The bits and bytes that are on hold when bit I2CHold is set to logic 1 are:

- MPIPON, SPIPON, DNonint and PipMode
- SHBlow and SVBlow
- SHRed and SVRed
- BGHfp and BGVfp
- SDHfp and SDVfp
- SHPic and SVPic
- BGOn, BOn and Prio
- BSel, SBBrt and SBCol
- SDSel
- MDHfp and MDVfp
- HBWidth and VBWidth.

SV1

Bit SV1 controls the internal horizontal offset of the background. When set to logic 0, the offset is 0.86 μs; when set to logic 1, the offset is 4.56 μs.

SV2

When set to logic 0, bit SV2 limits the range of the MAHfp and SAHfp parameters. Otherwise (bit SV2 set to logic 1), the parameters have their maximum range (which is recommended).

HBWIDTH AND VBWIDTH

Bits HBWidth<2:0> and VBWidth<2:0> control the horizontal and vertical border sizes in steps of two pixels and one line. The default horizontal border size is four pixels and the vertical border size is two lines per field. Default means after power-up and no I2C-bus data sent to the PIP controller.

In MP6 mode, the minimum value of HBWidth is two.

NOTES

1. When the input signals for the main and/or subchannel are non-interlaced, joint line errors can occur. When non-interlaced signals are input, the SAB9082 switches automatically to the non-interlaced mode.

2. When the prevent joint line error algorithm is switched off (AlgOff is set to logic 1), joint line errors can still occur in the 2-Field mode.

Acquisition channel ADCs and clamping

The analog input signals are converted to digital signals by three ADCs per channel. The resolution of the ADCs is 8 bits (DNL is 7 bits and INL is 6 bits) and the sampling is performed at the system clock frequency of 28 MHz for the Y input. A bias voltage (V_{bias}) is used to decouple the AC components on internal references.

The inputs should be AC coupled and an internal clamp circuit (using external clamp capacitors) will clamp the input to a level derived internally from $V_{ref(B)(MA/SA)}$ for the luminance channels and, for the chrominance channels, to $(V_{ref(T)(MA/SA)} + V_{ref(B)(MA/SA)})/2 + LSB/2$. The clamping starts at the active edge of the burst key. Internal video buffers amplify the standard Y, U and V input signals to the correct ADC levels.

PLL

The PLL generates an internal system clock of $1792 \times f_{HSYNC}$, from the f_{HSYNC}, which is approximately 28 MHz.

DACs and video buffers

The 28 MHz digital video signals are fed to the 8-bit DACs that produce the required analog video signals. The video buffers amplify these signals prior to being fed to the output to drive another device.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.5	5.0	V
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	ambient temperature	0	70	°C
V_{esd}	electrostatic discharge handling	–	2	kV
$R_{th(j-a)}$	thermal resistance	–	45	K/W
P_{max}	maximum power dissipation	–	1.0	W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611, Part E"*, dated 14 December 1992.

ESD LEVELS

The standard ESD specification is JEDEC Class II (2 kV Human Body Model, 200 V Machine Model) unless indicated otherwise.

Table 5 ESD performance

PIN	SYMBOL	HUMAN BODY MODEL (V)	MACHINE MODEL (V)
68	FBL	1000	standard specification
69	PKOFF	1000	
70	DVSYNC	1000	
72	SVSYNC	1000	
73	SCL	1000	
74	SDA	1000	
rest in range 1 to 17	all other pins	standard specification	
rest in range 64 to 100			

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ANALOG CHARACTERISTICS

V_{DDA} = 3.3 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	positive supply voltage		3.0	3.3	3.6	V
V_{SSA}	ground voltage		–	0	–	V
$\Delta V_{DDA(max)}$	maximum DC difference between supply voltages		–	0	100	mV
$\Delta V_{SSA(max)}$	maximum DC difference between ground voltages		–	0	100	mV
$I_{DDD(q)}$	quiescent current of digital supply voltages	note 1	–	0	50	μA
$I_{DDA(DP)}$	display PLL supply current		–	0.4	–	mA
$I_{DDA(SP)}$	sub PLL supply current		–	0.4	–	mA
$I_{DDA(MA)}$	main ADCs supply current	note 2	60	70	90	mA
$I_{DDA(SA)}$	sub ADCs supply current	note 2	60	70	90	mA
$I_{DDA(DA)}$	DACs supply current		8	10	12	mA
$I_{DDA(MF)}$	main buffers supply current		4	6	9	mA
$I_{DDA(SF)}$	sub buffers supply current		4	6	9	mA
$I_{DDA(tot)}$	total analog supply current	note 2	140	165	210	mA
$I_{DDD(tot)}$	total digital supply current		–	50	–	mA
Analog-to-digital converter and clamping						
$V_{ref(T)}$	top reference voltage	note 3	2.70	2.82	2.95	V
$V_{ref(B)}$	bottom reference voltage	note 3	0.95	1.07	1.20	V
$V_{iY(p-p)}$	Y input signal amplitude (peak-to-peak value)	note 4	–	1.00	1.04	V
$V_{i(V)(p-p)}$	V input signal amplitude (peak-to-peak value)	note 4	–	1.05	1.10	V
$V_{i(U)(p-p)}$	U input signal amplitude (peak-to-peak value)	note 4	–	1.33	1.38	V
I_i	input current	clamping off	–	0.1	–	μA
		clamping on	–	55	–	μA
C_i	input capacitance		–	5	–	pF
f_{sample}	sample frequency	note 5	–	$1792 \times f_{HSYNC}$	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		–1.4	–	+1.4	LSB
INL	integral non-linearity		–2.0	–	+2.0	LSB
α_{cs}	channel separation		–	48	–	dB
$V_{clamp(Y)}$	Y clamping voltage level	note 6	1.25	1.34	1.45	V
$V_{clamp(U,V)}$	U/V clamping voltage level	note 7	1.80	1.93	2.15	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter and output stage						
$V_{ref(T)}$	top reference voltage		1.10	1.20	1.30	V
$V_{ref(B)}$	bottom reference voltage		0.15	0.23	0.30	V
R_L	load resistance		1	–	1000	kΩ
C_L	load capacitance		0	–	5	pF
f_{sample}	sample frequency	note 8	–	$1792 \times f_{HSYNC}$	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		−1.0	–	+1.0	LSB
INL	integral non-linearity		−1.0	–	+1.0	LSB
α_{cs}	channel separation		–	48	–	dB
Display PLL and clock generation						
$f_{i(PLL)}$	input frequency	NTSC	14	15.75	17	kHz
Sub PLL and clock generation						
$f_{i(subPLL)}$	input frequency	NTSC	14	15.75	17	kHz

Notes

1. Digital clocks are silent, input pins POR and TM are connected to V_{DDA}.

2. This value is measured with an external bias resistor of 39 kΩ resulting in a bias current of 55 μA.

3. Voltages $V_{ref(T)}$ and $V_{ref(B)}$ are made by a resistor division of V_{DDA}. They can be calculated with the formulas:

$$V_{ref(T)} = V_{DDA} \times \frac{2.82}{V_{DDA(nom)}} V \text{ and } V_{ref(B)} = V_{DDA} \times \frac{1.07}{V_{DDA(nom)}} V .$$

4. The input signals are amplified to meet an internal peak-to-peak voltage level of $0.8 \times (V_{ref(T)} - V_{ref(B)})$, which equals the internal ADC input range.

5. The internal system clock frequency is $1792 \times f_{HSYNC}$ of the input channel.

6. The clamp level is not equal to the $V_{ref(B)}$ of the ADCs.

7. The UV channels are clamped to: $\dfrac{V_{ref(B)} + V_{ref(T)} + V_{LSB}}{2}$.

8. The internal system clock frequency is $1792 \times f_{HSYNC}$ of the main channel.

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DIGITAL CHARACTERISTICS

V_{DDA} = 3.3 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics						
V_{IH}	HIGH-level input voltage					
	default		$0.8V_{DDD}$	–	V_{DDD} + 0.5	V
	pin 74		$0.8V_{DDD}$	–	5.5[1]	V
	5 V tolerant pins 68, 69, 70, 72, 73		$0.8V_{DDD}$	V	5.5[1]	V
V_{IL}	LOW-level input voltage	default	−0.5	–	$0.2V_{DDD}$	V
V_{hys}	hysteresis voltage		0.8	–	–	V
V_{OH}	HIGH-level output voltage	I_{OH} = −X mA; V_{DDD} = 3.0 V; note 2	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = X mA; V_{DDD} = 3.0 V; note 2	–	–	0.4	V
		I_{OL} = 2 mA; V_{DDD} = 3.0 V	–	–	0.4	V
$|I_{LI}|$	input leakage current	V_I = 0 V	–	–	1	μA
		V_I = V_{DDD}	–	–	1	μA
$|I_{OZ}|$	3-state output leakage current	V_O = 0 V or V_O = V_{DDD}	–	–	1	μA
$I_{lu(I/O)}$	I/O latch-up current	V < 0 V; V > V_{DDD}	200	–	–	mA
R_{pu}	internal pull-up resistor		16	33	78	kΩ
AC characteristics						
$f_{clk(sys)}$	system clock frequency	note 3	–	1792 × f_{HSYNC}	–	kHz
t_r	rise time		–	6	25	ns
t_f	fall time		–	6	25	ns

Notes

1. The absolute maximum input voltage is 6.0 V.

2. X is the source/sink current under worst case conditions. X is reflected in the name of the I/O cell according to the drive capability. The minimum value of X is 1 mA.

3. The internal system clock frequency is 1792 × f_{HSYNC} of the main channel and subchannel.

TEST AND APPLICATION INFORMATION

Figure 5 gives the application diagram in a standard configuration. Input signals main channel CVBS and subchannel CVBS from different video sources are processed by the SAB9082 and inserted by the YUV to RGB switch.
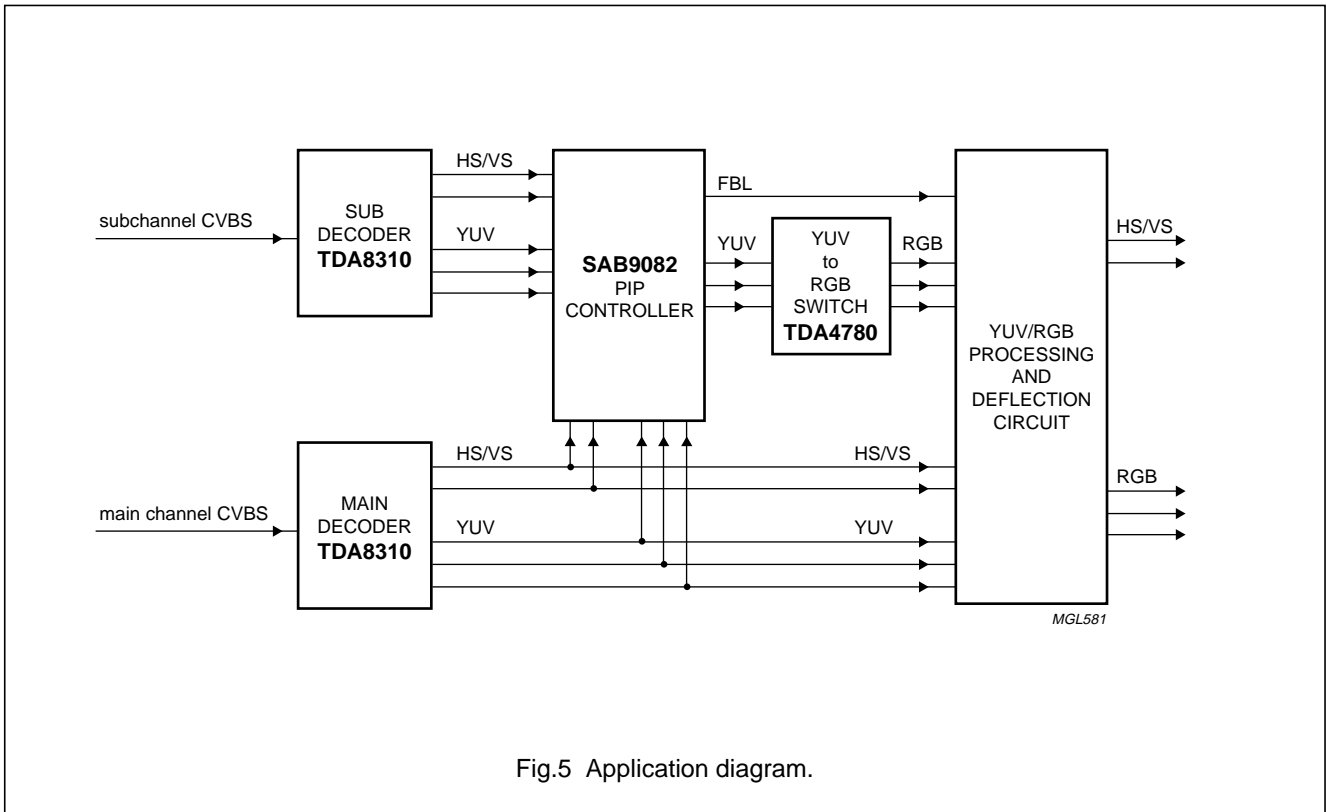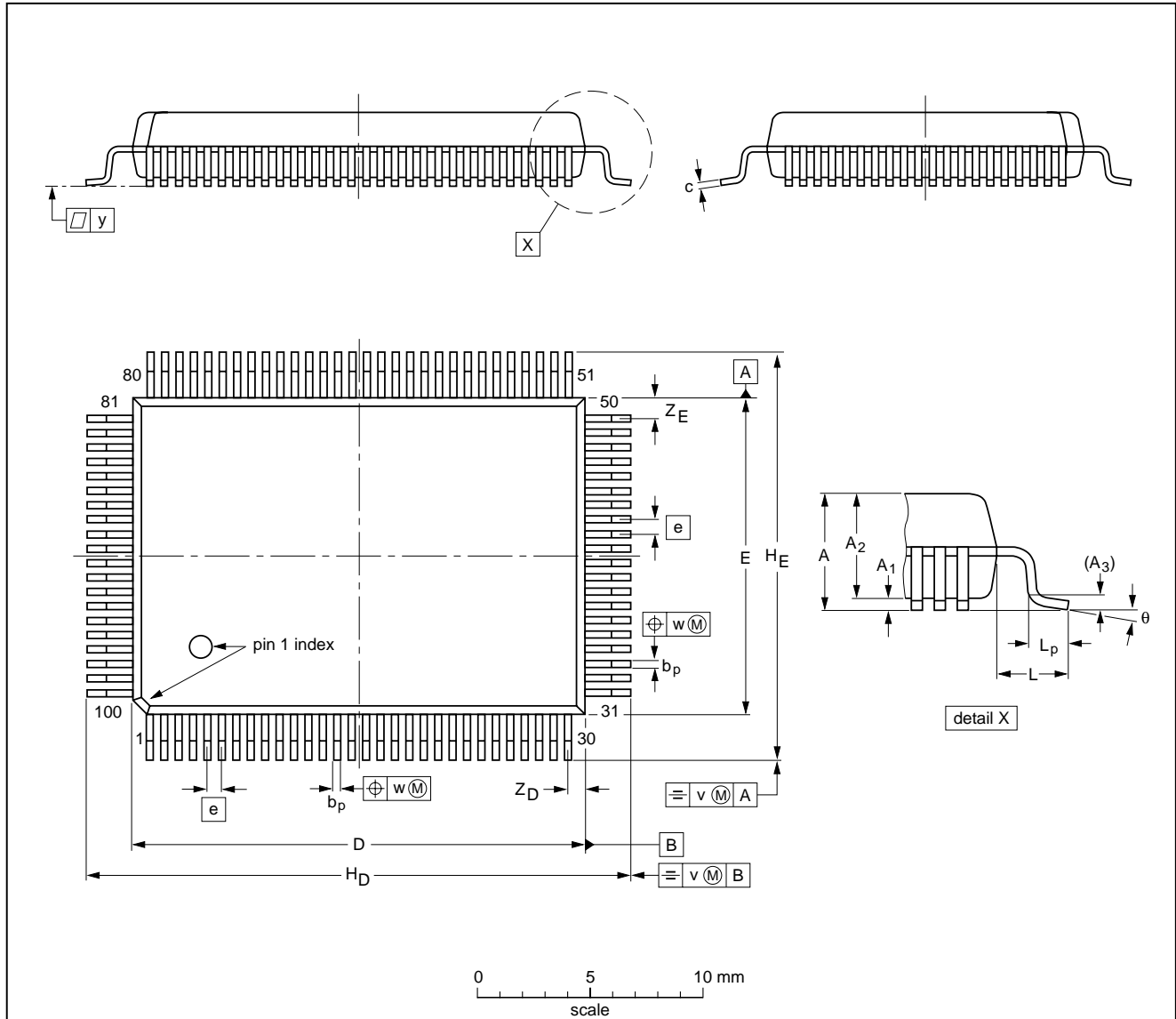

Fig.5 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm   **SOT317-2**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(1)}$	e	H$_D$	H$_E$	L	L$_p$	v	w	y	Z$_D^{(1)}$	Z$_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

NTSC Picture-In-Picture (PIP) controller

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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